EE 230
Fall 2006
Experiment 13

Data Converters – Performance Limitations associated with Nonideal Properties

Special Instructions for this Experiment

Since this experiment will be conducted during the last week of the semester, a report for this project will be turned in at the end of the period. There are 3 procedures listed for this experiment. You are to work sequentially on these procedures for the first 2 hours and 30 minutes of the lab period. At that time, you are to inform the TA exactly where you are in the measurements. The last 30 minutes are to be spent preparing a brief report which will be collected at the end of the laboratory period. Grades will be based upon how much progress you make on this experiment and on the brief report. Reports will only be accepted at the end of the laboratory period. If for any reason you can not spend the 3 scheduled hours working on this experiment, make arrangements in advance with your TA to attend a separate period.

Purpose: The purpose of this experiment is to investigate some of the limitations of data converters associated with nonideal properties of data converters. In particular, the issue of linearity as characterized by the integral nonlinearity (INL), the differential nonlinearity (DNL) and the spectral performance as characterized by the spurious free dynamic range (SFDR) will be explored.

Equipment:
Computer with MATLAB software
Data from Part 4 and Part 5 of Experiment 9

Background:

Data converters are widely used as the interface between the analog environment and the digital world. Analog to Digital Converters (ADC) convert physical analog signals to digital form and Digital to Analog Converters (DAC) convert digital signals analog form. In most applications, it is expected that all information about the input signal to an ADC be preserved in the sampled outputs obtained from the ADC. Correspondingly, it is generally expected that the output of a DAC will create the desired analog signal.

Existing data converters can come very close to accomplishing these tasks provided that the right data converter is used and provided it is used properly. Even if data converters are ideal, some potential problems can occur if the resolution is not high enough or if the sampling rates are too low. In some applications, the phase of the sampling clock is also very important. Inherent limitations associated with the data conversion process associated with ideal data converters were considered in the previous experiment.

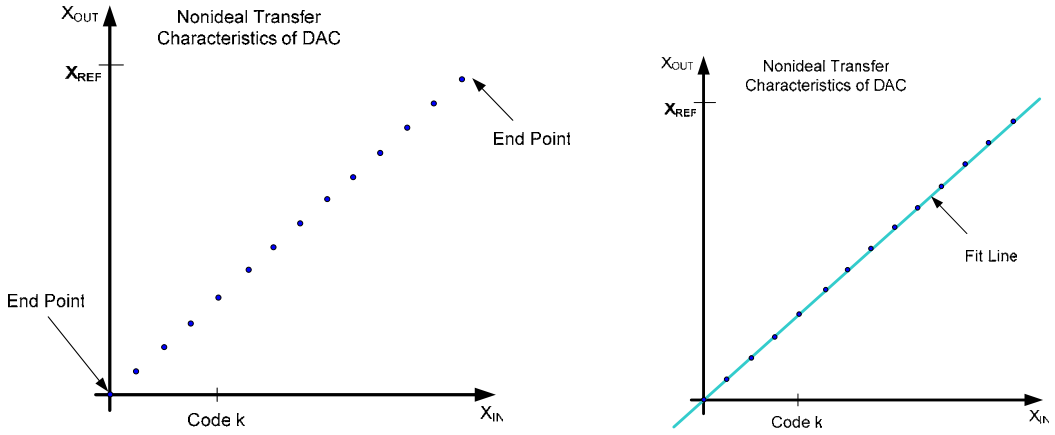
In this experiment, emphasis will be placed upon the performance capabilities and limitations associated with nonideal properties of data converters. The nonideal

properties of data converters are analogous to the nonideal properties of operational amplifiers such as finite GB, finite gain, offset voltage, and output saturation considered in previous laboratory experiments.

Linearity is one of the most important properties of data converters in many applications. If the output levels of a DAC are not uniformly spaced or if the transition points of an ADC are not uniformly spaced, the data converter will introduce nonlinearities into the output of the device that were not present in the input. These nonlinearities can affect the dc transfer characteristics of a system using the data converters and in such cases the parameters that the data converter that are of most concern are the integral nonlinearity (INL) and the differential nonlinearity (DNL). They can also affect the spectral performance of a system and in such cases the spectral performance as characterized by the total harmonic distortion (THD) and the spurious free dynamic range (SFDR) of the data converter are of most concern. In this experiment the INL, DNL, and SFDR will be considered.

Integral and Differential Nonlinearity

The transfer characteristics of an ideal DAC are shown in Fig. 1a. Note that the output for the smallest Boolean input corresponds to $X_{OUT}=0$ and the output corresponding to the largest Boolean input is close to X_{REF}. More importantly, note that all transition points are co-linear. The two extreme points are called the end points. A fit line that goes through all output points of the DAC is shown in Fig. 1b.



(a) (b)

Fig. 1 Transfer Characteristics of an ideal DAC

Other ideal transfer characteristics are also possible but the key property of the ideal transfer characteristics is that the outs of the DAC all lie on a straight line.

The transfer characteristics of a nonideal DAC are shown in Fig. 2a It can be observed that the transfer characteristics do not lie on a straight line. The linearity characteristics of a DAC are often defined relative to a fit line to the actual outputs of the DAC. There are many different fit lines that could be used but the data converter community generally used the end-point fit line. The end-point fit line is the line that

goes through the two extreme points in the dc transfer characteristics and is shown in Fig. 2b. Note this fit line does not go through the origin and does not have the same slope as that of the ideal fit line of Fig. 1b. The offset from passing through the origin is termed an offset error and the change in slope from that of the ideal DAC is termed a gain error.

The deviation of the actual output from the end-point fit-line output at code k is defined to be the INL at that code, that is,

$$INL_k = X_{OUT}(k) - X_{FIT}(k). \quad (1)$$

The overall INL is defined to be the maximum over k of the magnitude of all of the INL_k terms, that is,

$$INL = \max_{1 \le k \le N} \left\{ \left| INL_k \right| \right\} \quad (2)$$

where N is the total number of DAC input codes. The location where the deviation is maximum in the DAC of Fig. 2a is shown in Fig. 2b and designated as INL.
The INL is often designated relative to an LSB by dividing the INL by X_{LSB}. Thus, an n-bit ADC with a reference of X_{REF} has an LSB of $X_{REF}/2^n$ so the INL becomes

$$INL_{LSB} = \frac{INL}{X_{LSBF}} \quad (3)$$

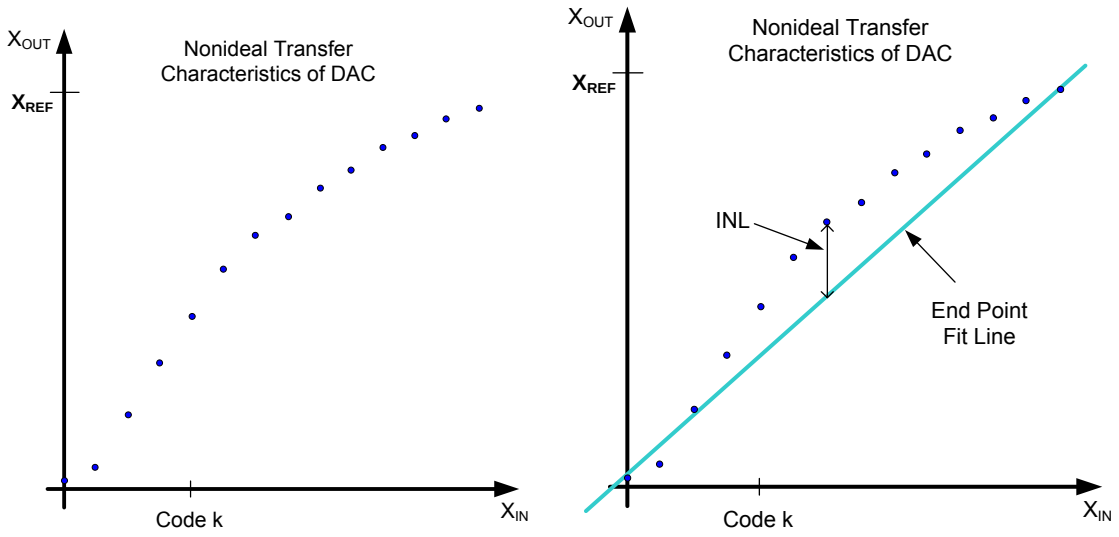
where X_{LSBF} is given by

$$X_{LSBF} = \frac{X_{OUT}(N) - X_{OUT}(1)}{N-1} \quad (4)$$

The term X_{LSBF} is approximately $X_{REF}/2^n$ and the distinction between these two terms which are very close is often not made and thus the INL is often expressed as

$$INL_{LSB} \cong 2^n \frac{INL}{X_{REF}} \quad (5)$$

Often the LSB subscript is omitted and it is assumed that the reader can correctly distinguish between I_{NL} and INL_{LSB} from the context in which the specification is given.



(a) (b)

Fig. 2 Transfer Characteristics of nonideal DAC

The differential nonlinearity, DNL, at code k is defined to be the difference between the increase in the output at code k to that of code k-1 and the ideal increase relative to the fit line. That is,

$$DNL_k = X_{OUT}(k) - X_{OUT}(k-1) - X_{LSBF} \tag{6}$$

and, as before, it is often assumed that $X_{LSBF}=X_{LSB}$.

The overall DNL is defined to be the maximum over all increments of the magnitude of the DNL_k terms. That is,

$$DNL = \max_{1<k\leq N} \{|DNL_k|\} \tag{7}$$

Since there are N-1 increments, note the lower limit on the range for DNL starts with index k=2.

The definitions for the INL and the DNL for an ADC are very similar. The number of transition points for an ADC is 1 less than the number of Boolean outputs for the ADC. Thus, if an ADC has N Boolean outputs (generally $N=2^n$ where n is the number of bits of resolution of the ADC) , there will be N-1 transition points. These transition points can be designated as $X_1, \ldots X_{N-1}$. The INL_k for an ADC is defined to be the difference between the kth transition point and the kth uniformly-spaced transition point between the first and last transition points. The uniformly spaced transition points between the first and last transition point represent an end-point fit-line to the transition points. If this point is designated as $X_{FIT}(k)$, the INL_k can be expressed as

$$INL_k = X_{TRANS}(k) - X_{FIT}(k) \tag{8}$$

It can be readily shown that the fit line is given by the expression

$$X_{FIT}(k)=X_{TRANS}(1)+\left(\frac{k-1}{N-2}\right)\frac{X_{TRANS}(N-1)-X_{TRANS}(1)}{N-2} \qquad (9)$$

for $1\leq k\leq N-1$.

The DNL for a transition point k of an ADC is defined to be the difference between the actual increment from transition point k-1 and the uniformly spaced increment. This is approximately given by the expression

$$DNL_k \cong X_{TRANS}(k)-X_{TRANS}(k-1)-X_{LSB} \qquad (10)$$

And, as for the DAC, the DNL for an ADC is defined to be

$$DNL = \max_{1<k\leq N}\left\{\left|DNL_k\right|\right\} \qquad (11)$$

Equivalent Number of Bits

If the transfer characteristics of an ADC do not lie on a straight line, the effects to the errors on a circuit using the data converter may be similar to those introduced by an ADC with less resolution. The equivalent number of bits (ENOB) is used to characterize the linearity performance of a data converter. The ENOB that is used to characterize the linearity of a data converter should not be confused with the ENOB used to characterized the signal to noise ratio (SNR) discussed earlier in this course.

Either a DAC or an ADC with n-bits of resolution should ideally be able to ideally represent a signal to within ± ½LSB for any input and should be able to represent the signal perfectly at the output points for a DAC or at the transition points for an ADC. As such, it will be assumed that ± ½LSB deviation from the ideal output or form the transition points is acceptable for an n-bit data converter but a larger deviation represents an effective degradation in resolution. With this understanding, an n-bit data converter with an INL of 1 LSB would be performing as if it were an n-1 bit data converter, one with an INL of 2 LSB would be performing at is it were an n-2 bit converter, one with an INL of 4 LSB would be performing as if it were an n-3 bit converter, etc. Mathematically the ENOB for a data converter with n bits of resolution and an INL of υ LSB can thus be expressed as

$$ENOB = n-1-\frac{\log_{10}\nu}{\log_{10}2} \qquad (12)$$

Spectral Characterization

Any nonlinearities in the transfer characteristics of a data converter will affect the spectral performance of the data converter. Specifically, if a sinusoidal input is applied to the data converter, harmonic components will be present in the output.

For example, if the input to a data converter is

$$X_{IN}=X_M\sin(\omega t+\theta) \tag{13}$$

then the interpreted output will be of the form

$$X_{OUT}=A_0+A_1\sin(\omega t+\theta+\gamma_1)+\sum_{k=2}^{\infty}A_k\sin(k\omega t+\theta+\gamma_k) \tag{14}$$

where Ak is the magnitude of the kth harmonic component of the ouput. The terms in the right summand represent spectral distortion and is comprised of frequency components that are not present in the input signal. The THD is generally defined to be the total power in the second and higher harmonic terms relative to the power in the fundamental. That is,

$$THD=\frac{\sum_{k=2}^{\infty}A_k^2}{A_1^2} \tag{15}$$

This is often expressed in decibels as

$$THD_{dB}=10\log_{10}\left(\frac{\sum_{k=2}^{\infty}A_k^2}{A_1^2}\right) \tag{16}$$

Generally the contributions by the higher-order terms is negligible and the sum can be made over only the first few terms.

A second metric is often used to characterize the spectral performance and that is the spurious free dynamic range (SFDR). The SFDR is defined to be

$$SFDR=\frac{|A_1|}{\max_{1<k}\{|A_k|\}} \tag{17}$$

Usually the SFDR is expressed in dB as given by the expression

$$SFDR_{dB}=20\log_{10}\left(\frac{|A_1|}{\max_{1<k}\{|A_k|\}}\right) \tag{18}$$

The THD and the SFDR are generally measured by applying a sinusoidal excitation of near full-scale and then taking a large number of samples of the output waveform. From these samples, a Fourier Series representation of the output can be obtained and this Fourier Series representation is essentially that given in (14). The

following theorem provides a practical method for obtaining the Fourier Series representation of a signal x(t) from samples of the signal.

Theorem: If a periodic signal x(t) with period T=1/f is band-limited to frequency hf and if the signal is sampled N times over an integral number of periods, N_P, then

$$|A_m| = \frac{2}{N}\left|X(mN_P+1)\right| \qquad \textbf{for } 0 \le m \le h\text{-}1$$

where $\left\langle X(k)\right\rangle_{k=1}^{N-1}$ **is the DFT of the sampled sequence** $\left\langle x(kT_S)\right\rangle_{k=1}^{N-1}$ **where T_S is the sampling period.**

The sampling period is thus given by $T_S = \frac{T \bullet N_P}{N}$. Thus, if x(t) is band-limited to hf, the magnitude of the coefficients of the Fourier Series Representation A_0, A_1, A_2, A_3, … are the magnitudes of the DFT elements X(0), X(N_P+1), X(2N_P+1), X(3N_P+1), … The Fast Fourier Transform (FFT) is a computationally efficient way for calculating the DFT, particularly when the number of samples is a power of 2. The FFT is a routine that is available in MATLAB.

Generally a prime number of periods of the input signal are sampled. It is critical that the hypothesis of the theorem be satisfied, that is, that the signal is sampled precisely over an integral number of periods of the excitation. Even a very small skew in the sampling requirements will cause major problems with using the DFT to obtain the Fourier Series coefficients.

Part 1 INL ,DNL, and ENOB measurement of DAC

Determine the INL, DNL and the ENOB of the DAC you designed and tested in Experiment 9. Note that the ENOB can actually be larger than the resolution if the output values of the DAC have a very uniform spacing.

Part 2 INL ,DNL, and ENOB measurement of ADC

Determine the INL, DNL and the ENOB of the ADC you designed and tested in Experiment 9. Note that the ENOB can actually be larger than the resolution if the output values of the DAC have a very uniform spacing.

Part 3 Spectral Characterization

We do not have the test equipment needed to gather samples from the output of a DAC or an ADC with sufficient accuracy to do good spectral characterization of a high-resolution DAC or ADC at this time. So, we will assume that you have an ADC with X_{REF} = 1V and a sinusoidal input signal of angular frequency 1K rad/sec was applied with a 0-P amplitude of 0.49V. Assume the output waveform of the ADC was a sampled version of the signal

$X_{OUT}(t)=0.45\sin(1000t)+ 0.0002\sin(2000t)+0.00005\sin(3000t)$.

Assume that 4096 samples of this output were taken over precisely 11 periods of the input.

a) What is the THD of the output signal
b) What is the SFDR of the output signal
c) Determine the SFDR from Matlab and compare with the results obtained in part b)
d) (Ex cr) Determine the SFDR from Matlab if the sampled signal is quantized to the 12-bit level.